ing region may electrically be connected to the first interconnection in the potential fixing region extension portion. The gate electrode may electrically be connected to the second interconnection in the gate electrode extension portion.

[0014] The semiconductor device above may further include a second insulating film arranged above the potential fixing region and a second interconnection arranged above the second insulating film. The first interconnection may include a first interconnection extension portion extending beyond the outer peripheral trench to the potential fixing region. The second interconnection may include a second interconnection extension portion extending beyond the outer peripheral trench to the gate electrode. The first interconnection may electrically be connected to the potential fixing region in the first interconnection extension portion. The second interconnection may electrically be connected to the gate electrode in the second interconnection extension portion.

[0015] By doing so, electrical connection between the second interconnection arranged above the potential fixing region and the gate electrode can readily be achieved while a potential of the potential fixing region is fixed to the potential of the first interconnection.

[0016] In the semiconductor device above, an angle formed between a sidewall surface of the trench and one main surface may be from 100° to 160°. By thus gently forming a sidewall surface of the trench, electric field concentration around a trench bottom can be suppressed. It is noted that an angle formed between a sidewall surface of the trench and one main surface means an angle formed between a sidewall surface of the trench and one main surface in the semiconductor substrate.

[0017] In the semiconductor device above, the semiconductor substrate may be composed of silicon carbide. Thus, the semiconductor device according to the present invention can suitably be employed in a silicon carbide semiconductor device having the semiconductor substrate composed of silicon carbide.

[0018] A method of manufacturing a semiconductor device according to the present invention includes the steps of preparing a semiconductor substrate including a drift layer having a first conductivity type and a body layer having a second conductivity type, which is formed on the drift layer to include one main surface, forming a trench to open on a side of one main surface and to penetrate the body layer and reach the drift layer, forming a first insulating film to include a wall surface of the trench, forming a gate electrode to be in contact with the first insulating film, and forming a first interconnection on one main surface. In the step of forming a trench, an outer peripheral trench arranged to surround an active region when viewed two-dimensionally is formed. In the step of forming a first interconnection, the first interconnection is formed to lie over the active region when viewed two-dimensionally and to electrically be connected to a potential fixing region which is the body layer exposed at one main surface opposite to the active region when viewed from the outer peripheral trench.

[0019] According to the method of manufacturing a semiconductor device of the present invention, the semiconductor device according to the present invention above, in which a potential at a surface portion of a semiconductor layer located outside an active region is fixed, can be manufactured.

[0020] In the method of manufacturing a semiconductor device above, in the step of forming a trench, the outer peripheral trench may be formed simultaneously with the trench other than the outer peripheral trench. Thus, the step above can more efficiently be performed.

[0021] The method of manufacturing a semiconductor device above may further include the step of forming an electric field relaxing region having the second conductivity type, which extends to be in contact with the outer peripheral trench in the drift layer and to reach the potential fixing region. In the step of forming an electric field relaxing region, the electric field relaxing region may be formed through ion implantation.

[0022] Thus, a semiconductor device capable of relaxing electric field applied to the first insulating film arranged on a wall surface of the outer peripheral trench can readily be manufactured.

[0023] In the method of manufacturing a semiconductor device above, in the step of preparing a semiconductor substrate, a semiconductor substrate composed of silicon carbide may be prepared. Thus, the method of manufacturing a semiconductor device according to the present invention can suitably be employed in a method of manufacturing a silicon carbide semiconductor device including a semiconductor substrate composed of silicon carbide.

[0024] As is clear from the description above, according to the semiconductor device of the present invention, breakdown voltage characteristics can be improved by fixing a potential at a surface portion of a semiconductor layer located outside an active region. In addition, according to the method of manufacturing a semiconductor device of the present invention, the semiconductor device according to the present invention above can be manufactured.

[0025] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. **1** is a schematic diagram showing a cross-sectional structure of a MOSFET along the line A-A in FIG. **4**.

[0027] FIG. **2** is a schematic diagram showing a cross-sectional structure of the MOSFET along the line B-B in FIG. **4**.

[0028] FIG. **3** is a schematic top view partially showing a structure of the MOSFET.

[0029] FIG. **4** is a schematic top view partially showing a structure of the MOSFET.

[0030] FIG. **5** is a flowchart schematically showing a method of manufacturing a MOSFET.

[0031] FIG. **6** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.

[0032] FIG. **7** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.

[0033] FIG. **8** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.

[0034] FIG. **9** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.

[0035] FIG. **10** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.

[0036] FIG. **11** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.

[0037] FIG. **12** is a schematic cross-sectional view for illustrating the method of manufacturing a MOSFET.